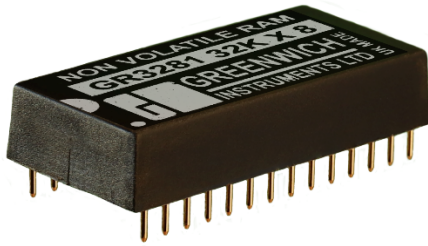


# NON-VOLATILE RAM

## GR3281 (32k X 8)



August 2025



### Description

The GR3281 is a 32768 word by 8 bits (32k x 8) non-volatile, advanced silicon gate, CMOS 70nS Static RAM IC with a high operational industrial temperature range. Memory contents are retained by the use of an internal, highly reliable, lithium power cell. Without any external power, the data retention is typically greater than ten years.

The pin-out of the device conforms to the JEDEC standards and is fully compatible with normal Static RAM. The power down circuit is fully automatic and is referenced at 4.5Vdc. At this point it is write-protected by an internal inhibit function for data protection and the memory contents are retained by the internal lithium cell.

Essential for data integrity, power down is very fast, less than 15µs from 5V to 0Vdc, faster than system power failure conditions.

### Application

When powered down, the device is transportable and the data contained can be moved from system to system making it ideal for program development, data collection in data-loggers, program changes in process control systems, automation and user-definable lookup tables etc.

### Absolute Ratings

SYMBOL	MIN	MAX	UNITS
V <sub>dd</sub>	-0.3	7.0	Vdc
V <sub>in/out</sub>	-0.3	V <sub>dd</sub> +0.3	Vdc
Temp	-40	+85	°C

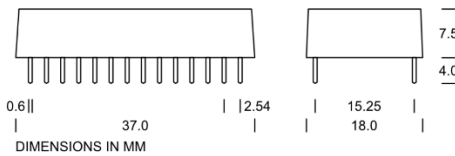
### Operating Conditions

SYMBOL	MIN	TYP.	MAX	UNITS
V <sub>dd</sub>	+4.75	+5.0	+5.5	Vdc
V <sub>in(1)</sub>	+2.2			Vdc
V <sub>in(0)</sub>			+0.8	Vdc
I <sub>in</sub> (any other pin)	-1.0		+1.0	µA
V <sub>out(1)</sub> (I <sub>out</sub> =-1mA)	+2.4			Vdc
V <sub>out(0)</sub> (I <sub>out</sub> =+2mA)			+0.4	Vdc
I <sub>dd(active)</sub>		30		mA
I <sub>dd(deselected)</sub>		1.0		mA
T <sub>cycle</sub>			70	nS
C <sub>in</sub> (any pin)		10		pF

### Pin Connections

Pin	Function
A14	A0-A14
A12	Data in/out
A7	Chip Enable
A6	Output Enable
A5	Chip Enable
A4	Output Enable
A3	Chip Enable
A2	Output Enable
A1	Chip Enable
A0	Output Enable
D0	D0-D7
D1	D0-D7
D2	D0-D7
D3	D0-D7
V <sub>dd</sub>	+5Volt Power
WR	Write Enable
OE	Output Enable
CE	Chip Enable
WE	Write Enable
D7	D0-D7
D6	D0-D7
D5	D0-D7
D4	D0-D7
D3	D0-D7
GND	Ground

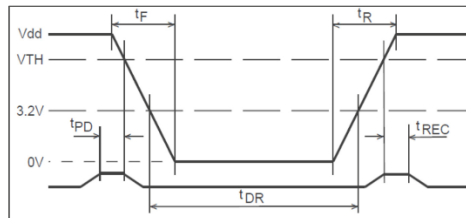
GREENWICH INSTRUMENTS GR3281 NON-VOLATILE RAM (32K X 8)



### Operating Mode

CE	OE	WR	MODE	OUTPUT	I <sub>dd</sub>
H	X	X	Unsel.	Hi-Z	Deselected
L	H	H	Unsel.	Hi-Z	Active
L	L	H	Read	Dout	Active
L	X	L	Write	Din	Active

### Data Retention Operating Conditions

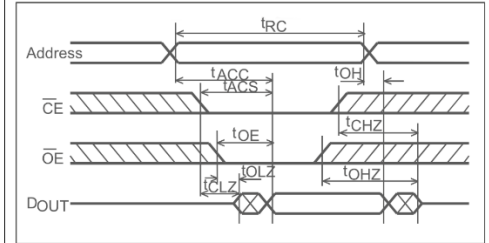


SYM	PARAMETER	MIN	TYP.	MAX	UNITS
V <sub>dd</sub>	Operating supply voltage	4.75	5.0	5.5	Vdc
V <sub>TH</sub>	Data retention voltage		4.5		Vdc
t <sub>F</sub>	V <sub>dd</sub> slew to 0V	15			µS
t <sub>R</sub>	V <sub>dd</sub> slew from 0V to 5V	15			µS
t <sub>REC</sub>	CE to O/P valid from power up			15	µS
t <sub>DR</sub>	Data retention time		10		Yrs.
t <sub>PD</sub>	CE at V <sub>in(1)</sub> before power down	0			µS

Please note:

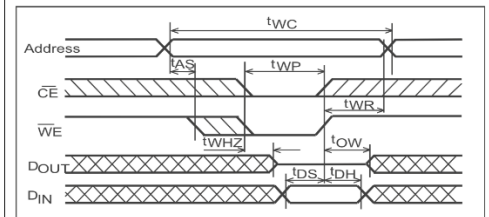
- WR must be high during address transitions
- A write occurs during the overlap of active CE and a low RW
- WR is high for a read cycle

### Read Cycle



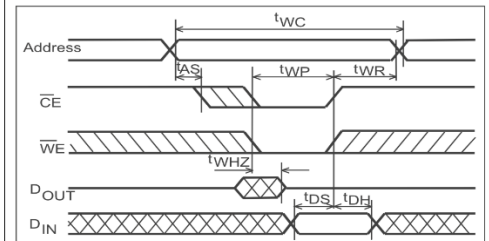
SYM	PARAMETER	MIN	MAX	UNITS
t <sub>RC</sub>	Read cycle time	70		nS
t <sub>ACC</sub>	Access time		70	nS
t <sub>ACS</sub>	CE to output valid		70	nS
t <sub>OE</sub>	OE to output valid		35	nS
t <sub>CLZ</sub>	CE to output active	10		nS
t <sub>OLZ</sub>	OE to output active	10		nS
t <sub>OH</sub>	Output hold time	10		nS
t <sub>CHZ</sub>	CE to output disable		25	nS
t <sub>OHZ</sub>	OE to output disable		25	nS

### Write Cycle 1



SYM	PARAMETER	MIN	MAX	UNITS
t <sub>WC</sub>	Write cycle time	70		nS
t <sub>WP</sub>	Write pulse width	50		nS
t <sub>AS</sub>	Address setup time	0		nS
t <sub>WR</sub>	Write recovery time	0		nS
t <sub>WHZ</sub>	WR to output disable		30	nS
t <sub>OW</sub>	Output active from WR	5		nS
t <sub>DS</sub>	Data setup time	30		nS
t <sub>DH</sub>	Data HOLD TIME	0		nS

### Write Cycle 2



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Do not dispose of non-volatile memory devices by incineration, crushing or landfill; devices can be returned, carriage paid, to Cephos Relays Limited for disposal

