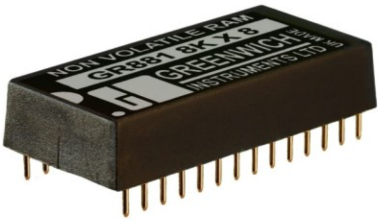
NON-VOLATILE RAM
GR881 (8k X 8)

CEPHOS RELAYS LIMITED

August 2025



Description

The GR881 is a 8192 word by 8 bits (8k x 8) non-volatile, advanced silicon gate, CMOS 70nS Static RAM IC with a high operational industrial temperature range. Memory contents are retained by the use of an internal, highly reliable, lithium power cell. Without any external power, the data retention is typically greater than ten years.

The pin-out of the device conforms to the JEDEC standards and is fully compatible with normal Static RAM. The power down circuit is fully automatic and is referenced at 4.5Vdc. At this point it is write-protected by an internal inhibit function for data protection and the memory contents are retained by the internal lithium cell.

Essential for data integrity, power down is very fast, less than 15μS from 5V to 0Vdc, faster than system power failure conditions.

Application

When powered down, the device is transportable and the data contained can be moved from system to system making it ideal for program development, data collection in data-loggers, program changes in process control systems, automation and user-definable lookup tables etc.

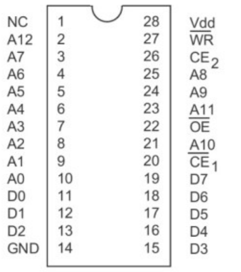
Absolute Ratings

SYMBOL	MIN	MAX	UNITS
Vdd	-0.3	7.0	Vdc
Vin/out	-0.3	Vdd+0.3	Vdc
Temp	-40	+85	ºC

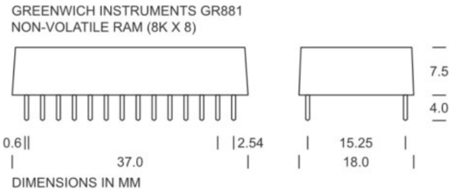
Operating Conditions

SYMBOL	MIN	TYP.	MAX	UNITS
Vdd	+4.75	+5.0	+5.5	Vdc
Vin(1)	+2.2		Vdd+0.3	Vdc
Vin(0)	-0.3		+0.8	Vdc
Iin (any other pin)	-1.0		+1.0	μA
Vout(1) (Iout=-1mA)	+2.4			Vdc
Vout(0) (Iout=+2mA)			+0.4	Vdc
Idd(active)		30		mA
Idd(deselected)		1.0		mA
Tcycle			70	nS
Cin(any pin)		10		pF

Pin Connections



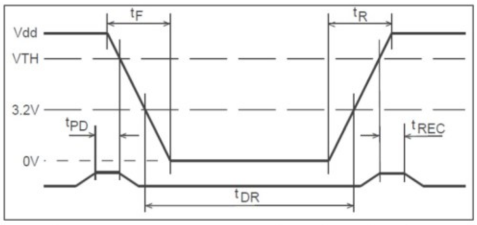
Pin	Function
A0-A12	Address I/P`s
D0-D7	Data in/out
$\overline{OE}$	Output Enable
$\overline{CE}_1$ CE_2	Chip Enable
$\overline{WR}$	Write Enable
Vdd	+5Volt Power
GND	Ground



Operating Mode

$\overline{CE}$	$\overline{OE}$	$\overline{WR}$	MODE	OUTPUT	Idd
H	X	X	Unsel.	Hi-Z	Standby
L	H	H	Unsel.	Hi-Z	Active
L	L	H	Read	Dout	Active
L	X	L	Write	Din	Active

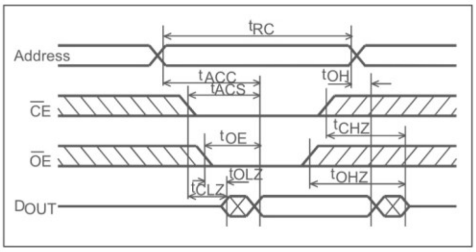
Data Retention Operating Conditions



SYM	PARAMETER	MIN	TYP.	MAX	UNITS
V_{dd}	Operating supply voltage	4.75	5.0	5.5	Vdc
V_{TH}	Data retention voltage		4.5		Vdc
t_F	V_{dd} slew to 0V	15			μS
t_R	V_{dd} slew from 0V to 5V	15			μS
t_{REC}	CE to O/P valid from power up			15	μS
t_{DR}	Data retention time		10		Yrs.
t_{PD}	CE at Vin(1) before power down	0			μS

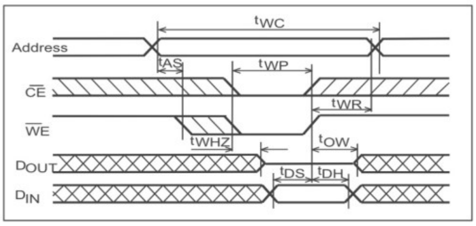
Please note:
1. WR must be high during address transitions
2. A write occurs during the overlap of active CE and a low WR
3. CE = CE1 and CE2
4. WR is high for a read cycle

Read Cycle



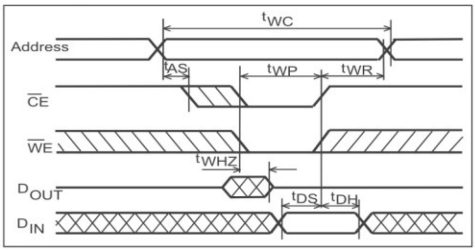
SYM	PARAMETER	MIN	MAX	UNITS
t_{RC}	Read cycle time	70		nS
t_{ACC}	Access time		70	nS
t_{ACS}	$\overline{CE}$ to output valid		70	nS
t_{OE}	$\overline{OE}$ to output valid		35	nS
t_{CLZ}	$\overline{CE}$ to output active	10		nS
t_{OLZ}	$\overline{OE}$ to output active	10		nS
t_{OH}	Output hold time	10		nS
t_{CHZ}	$\overline{CE}$ to output disable		25	nS
t_{OHZ}	$\overline{OE}$ to output disable		25	nS

Write Cycle 1



SYM	PARAMETER	MIN	MAX	UNITS
t_{WC}	Write cycle time	70		nS
t_{WP}	Write pulse width	50		nS
t_{AS}	Address setup time	0		nS
t_{WR}	Write recovery time	10		nS
t_{WHZ}	$\overline{WR}$ to output disable		20	nS
t_{OW}	Output active from $\overline{WR}$	5		nS
t_{DS}	Data setup time	30		nS
t_{DH}	Data HOLD TIME	0		nS

Write Cycle 2



Cephos Relays Limited
57 Devon Road
South Darenth
Dartford
Kent DA4 9AA
United Kingdom

Telephone: +44 (0)7540 777054
Email: sales@cephosrelays.com
https://cephosrelays.com

Do not dispose of non-volatile memory devices by incineration, crushing or landfill; devices can be returned, carriage paid, to Cephos Relays Limited for disposal

RoHS Compliant